

# A GaAs HBT MONOLITHIC MICROWAVE SWITCHED-GAIN AMPLIFIER WITH +31 dB TO -31 dB GAIN IN 2 dB INCREMENTS

A. K. Oki, G. M. Gorman, J. B. Camou, D. K. Umemoto, and M. E. Kim

TRW Inc., Electronics & Technology Division  
One Space Park, Redondo Beach, CA 90278

## ABSTRACT

A GaAs/AlGaAs heterojunction bipolar transistor (HBT) monolithic 5-bit digital gain control amplifier has been developed for application to electronic warfare receivers. The switched-gain/attenuator amplifier performance includes monotonic gain control in 2 dB increments from +31 dB to -31 dB from DC to 2.25 GHz with less than 1.6 dB RMS gain error across the band. The chip size is  $1.2 \times 2.2 \text{ mm}^2$  and consumes 1.3 watts. The circuit is the first reported monolithic microwave HBT gain control circuit for signal processing applications as well as one of the first three chips (all HBTs) demonstrated on the DARPA Microwave/Millimeter Wave Monolithic Integrated Circuit (MIMIC) Phase 1 Program.

## INTRODUCTION

Advanced electronic receivers need to process wide dynamic range signals over a wide frequency range. Switched gain/attenuator amplifiers are used to provide the appropriate receiver ranging capability. Previous approaches to microwave switched attenuators are implemented using dual-gate GaAs MESFETs with segmented transistor widths [1-3]. This topology results in a very compact layout and low power consumption, but is limited in its dynamic range and gain accuracy. The dynamic range is limited by the maximum possible ratio of transistor widths, while the gain accuracy is limited by device matching. Another approach to digital gain control parallels a shorting switch with a linear amplifier at each stage [4], but results in a relatively large circuit layout. The GaAs HBT with its intrinsic advantages over GaAs MESFETs and advanced Si bipolar offers an attractive alternative to variable gain amplifier application to increase the dynamic range of existing receiver systems and provide solutions for future wideband architectures.

## CIRCUIT DESIGN

The digital-control variable gain amplifier is composed of five gain/attenuation stages and an output buffer, as described in Fig. 1. A current-mode logic (CML) switch selects either the high gain differential pair or the attenuating differential pair for each of the

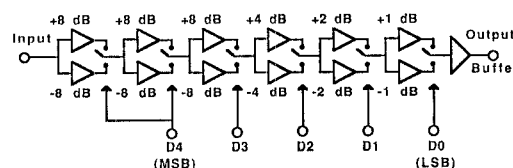


Fig. 1. Block Diagram of Five Bit Digital Gain Control Amplifier.

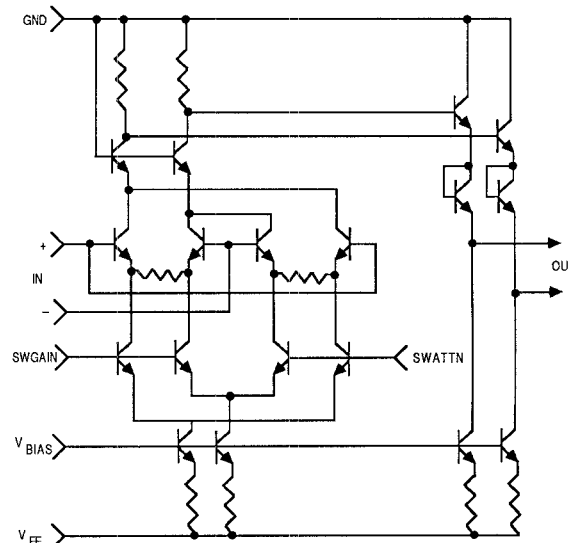


Fig. 2. Single Stage Schematic.

five stages shown in Fig. 2. Distributing the gain into  $\pm 16 \text{ dB}$ ,  $\pm 8 \text{ dB}$ ,  $\pm 4 \text{ dB}$ ,  $\pm 2 \text{ dB}$ , and  $\pm 1 \text{ dB}$  increments achieves the desired  $\pm 31 \text{ dB}$  programmability in 2 dB increments. The MSB gain stage ( $\pm 16 \text{ dB}$ ) is composed of two  $\pm 8 \text{ dB}$  stages. The gain or attenuation of each stage is determined by the ratio of the load resistance to the emitter resistance plus the emitter contact resistance and the dynamic emitter resistance. The larger the emitter resistance, the smaller the gain variation due to device variation, current bias, and

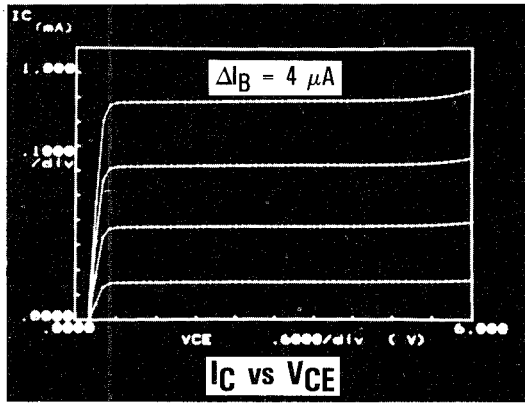


Fig. 3. GaAs HBT I-V Characteristics.

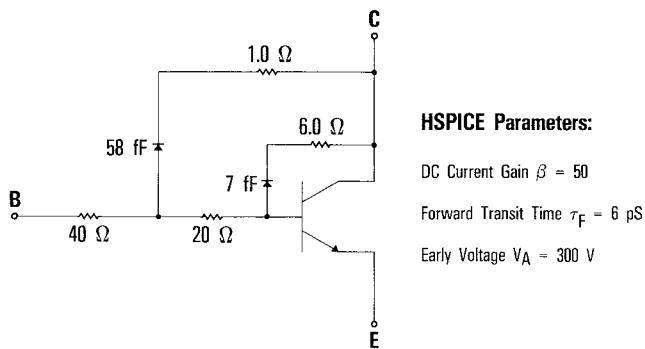


Fig. 4. GaAs HBT SPICE Model.

temperature. The circuit does not require backside ground vias, air bridges, or spiral inductors. Balanced differential pair amplifiers do not require a low impedance ( $< 0.5 \text{ nH}$ ) ground, unlike typical single-ended GaAs MESFET amplifiers. The DC-coupled design topology does not require spiral inductors for DC biasing (RF chokes). Monotonicity is insured by designing the gain/attenuation difference of each succeeding stage to be slightly greater than the sum of the preceding stages. Monotonicity over all operating conditions is a requirement of many system designs.

#### GaAs HBT IC FABRICATION

The switched gain amplifiers were fabricated with a  $3\text{-}\mu\text{m}$  emitter, self-aligned base ohmic metal (SABM) HBT IC fabrication process designed for baseband/RF analog applications, previously reported in detail [5]. The mesa HBT IC process incorporates Npn transistors, nichrome thin-film resistors, and metal-insulator-metal capacitors which are isolated using boron damage implantation and integrated using a double-level interconnect. Molecular-beam epitaxy is used for the HBT device structure. This process has already demonstrated state-of-the-art microwave amplifiers and oscillators [6]. DC current gain  $\beta \approx 50$  (Fig. 3) and high  $f_T$  and  $f_{\text{max}}$  (15-30 GHz) at low collector current density

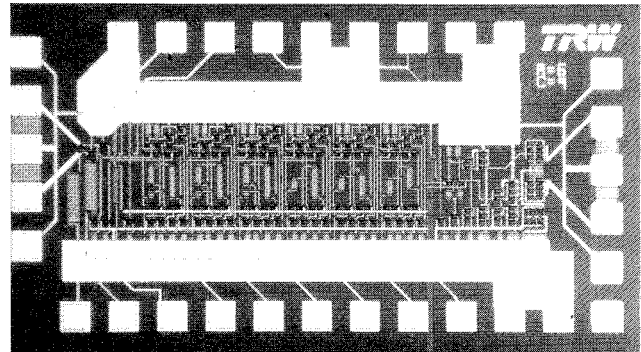


Fig. 5. Photomicrograph of GaAs HBT Switched Gain Amplifier (155 HBTs;  $2.1 \times 1.2 \text{ mm}^2$ ).

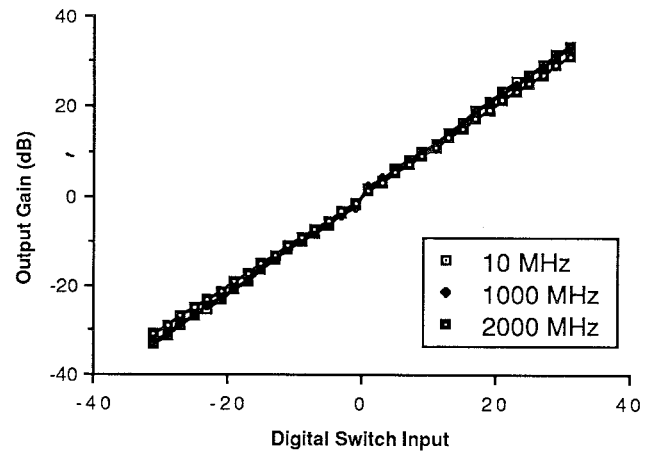


Fig. 6. Gain Versus Digital Switch Input (10, 1000, and 2000 MHz).

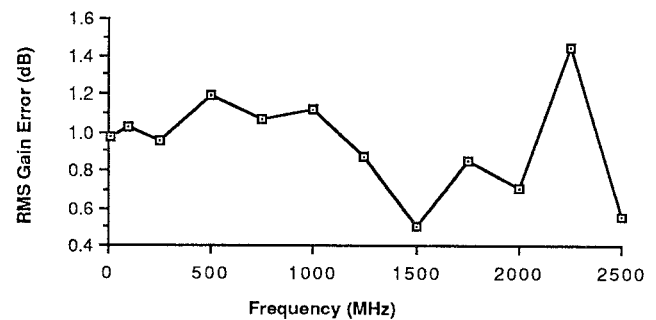


Fig. 7. Graph of RMS Integral Gain Error Versus Frequency.

$J_C \approx 3 \text{ kA/cm}^2$  combine to provide high accuracy RF/analog and high speed digital performance. The SPICE transistor model for the standard HBT, with a  $3 \times 10\text{-}\mu\text{m}^2$  emitter, is shown in Fig. 4.

The fabricated switched gain amplifier shown in Fig. 5 contains 155 HBTs and occupies a die size of  $2.1 \times 1.2 \text{ mm}^2$ .

## SWITCHED-GAIN AMPLIFIER PERFORMANCE

The switched-gain amplifier can be operated single-ended or differential on both input and output, however this work focused on single-ended input and output. All circuit testing was performed on-wafer using a ceramic blade microstrip probe card. The circuit consumes 1.3 watts (-8.5 V at 150 mA). Figure 6 gives the gain versus digital switch input at 10, 1000, and 2000 MHz. Figure 7 gives the frequency dependence of RMS gain error which is the RMS difference of the gain from a perfectly linear gain transfer function. Figure 8 shows all 32 five bit gain combinations versus frequency. Figures 9-12 show the inherent monotonicity of the circuit at 1 GHz with each photo showing 8 of the 32 bit patterns. Figure 13 shows the maximum gain +31 dB pattern and all five bit switches in attenuation, one at a time at 1 GHz. The -35 dBm (11 mV peak-to-peak) input signal is 1 dB more than the smallest input magnitude trace shown, which is in the -1 dB gain mode.

The circuit was tested from 10°C to 125°C. The gain in the maximum gain mode versus frequency and over the temperature range is shown in Fig. 14. At

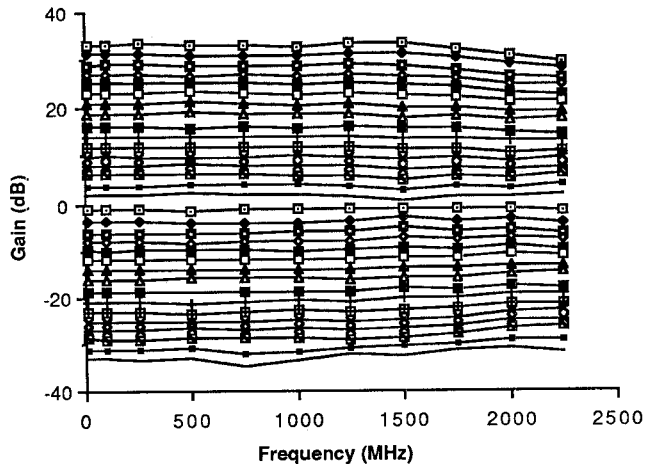


Fig. 8. Gain Versus Frequency For All 32 Gain Settings.

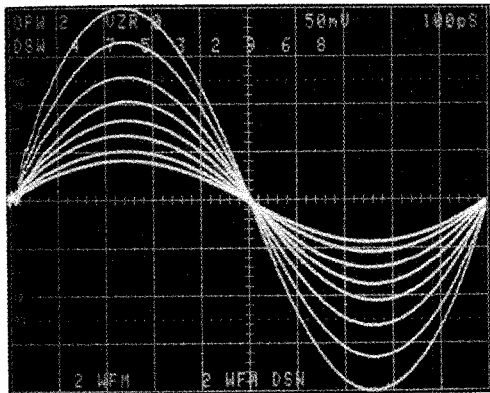


Fig. 9. Response of a -35 dBm 1 GHz Signal in the +31, +29, +27, +25, +23, +21, +19, and +17 dB Gain Settings (V: 50 mV/div; H: 100 pS/div).

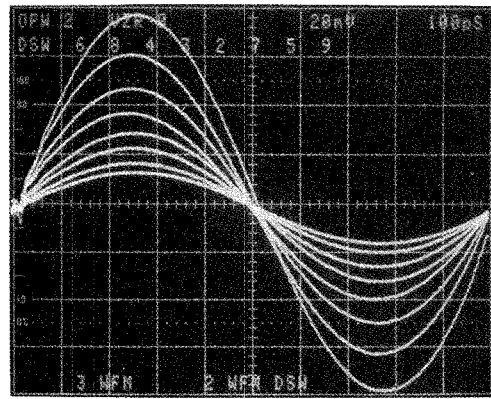


Fig. 10. Response of a -27 dBm 1 GHz Signal in the +15, +13, +11, +9, +7, +5, +3, and +1 dB Gain Settings (V: 20 mV/div; H: 100 pS/div).

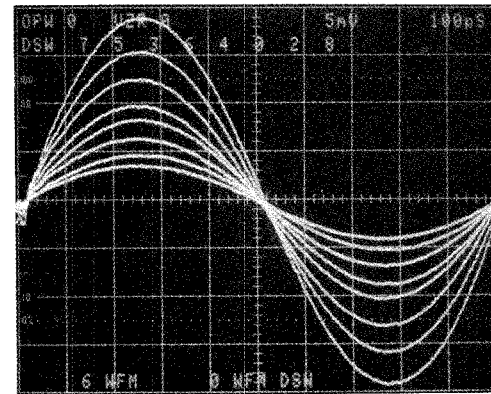


Fig. 11. Response of a -23 dBm 1 GHz Signal in the -1, -3, -5, -7, -9, -11, -13, and -15 dB Gain Settings (V: 5 mV/div; H: 100 pS/div).

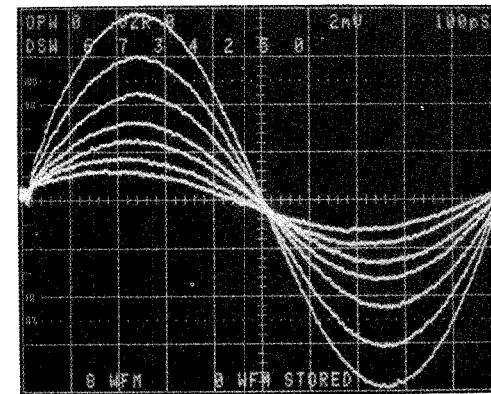


Fig. 12. Response of a -15 dBm 1 GHz Signal in the -17, -19, -21, -23, -25, -27, -29, and -31 dB Gain Settings (V: 2 mV/div; H: 100 pS/div).

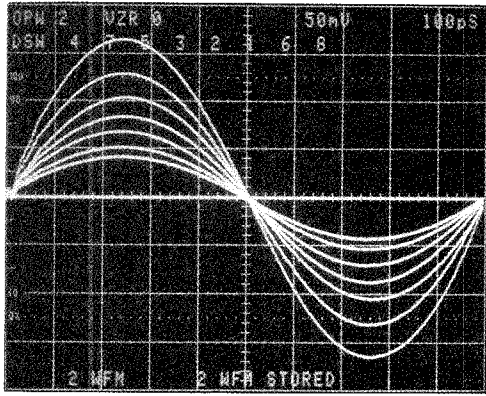


Fig. 13. Response of a -35 dBm 1 GHz Signal in the +31, +29, +27, +23, +15, and -1 dB Gain Settings (V: 50 mV/div; H: 100 pS/div)

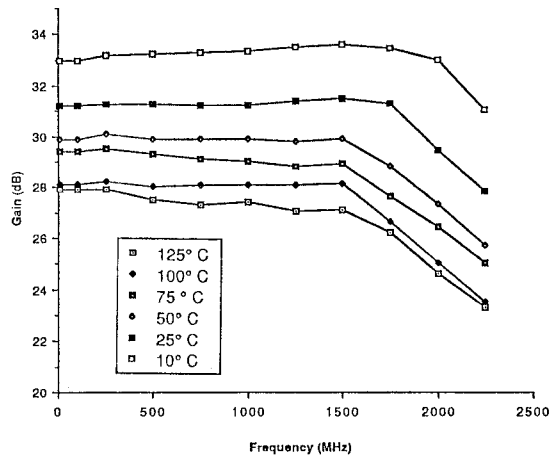


Fig. 14. Gain Versus Frequency At 10°C, 25°C, 50°C, 75°C, 100°C, and 125°C (Gain Setting is +31 dB).

room temperature the -3 dB frequency is 2.25 GHz. Without temperature compensation, the circuit has a maximum  $\pm 3$  dB gain variation window. Since the gain variation with temperature is well behaved, on-chip temperature compensation techniques should be adequate.

## SUMMARY AND CONCLUSION

GaAs HBTs have been used to fabricate a monolithic 5-bit control switched-gain amplifier for signal processing applications. The circuit has monotonic gain from +31 dB to -31 dB in 2 dB increments from DC to 2.25 GHz. The circuit has advantages over competing GaAs MESFET implementations in ease of design and fabrication.

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